

What is claimed is:

1. A method for making a bipolar transistor, comprising:
forming collector, base, and emitter semiconductor layers on a substrate, the
layers forming a vertical sequence with respect to an adjacent surface of the substrate;
etching away a portion of a top one of the semiconductor layers to expose a
5 portion of the base semiconductor layer, the top one of the semiconductor layers being
the layer of the sequence that is located farthest from the substrate; and
growing semiconductor on the exposed portion of the base layer such that a
vertical portion of the top one of the semiconductor layers is laterally surrounded by
the grown semiconductor.
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2. The method of claim 1, wherein the grown semiconductor has the same
conductivity type as the base layer.
3. The method of claim 1, further comprising:
15 forming a dielectric sidewall around the top one of the semiconductor layers
prior to performing the growing step.
4. The method of claim 3, further comprising:
forming a dielectric cap over the top one of the semiconductor layers prior
20 performing the growing step, the dielectric cap not being removed by the etching step.
5. The method of claim 1, wherein the growing step produces an extrinsic
portion of base layer, the extrinsic portion extending vertically farther from the
surface of the substrate than the top one of the semiconductor layers.
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6. The method of claim 1, wherein a bottom one of the semiconductor
layers is formed by implant doping a region of the substrate.
7. The method of claim 2, further comprising:

forming a semiconductor extension to the top one of the semiconductor layers such that a portion of the grown semiconductor is located between the extension and the substrate.

- 5 8. An integrated circuit, comprising:
a substrate having a planar surface;
collector, base, and emitter semiconductor layers of a bipolar transistor, the
semiconductor layers forming a vertical sequence on the substrate in which intrinsic
portions of two of the layers are sandwiched between the substrate and a remaining
10 top one of the layers; and
wherein the base layer comprises an extrinsic semiconductor extension that
laterally encircles a vertical portion of the top one of said semiconductor layers.
- 15 9. The apparatus of claim 8, further comprising:
a dielectric sidewall interposed between the vertical portion of the top one of
the layers and the extension of the base layer.
- 20 11. The apparatus of claim 8, wherein the extension of the base layer
extends farther away from the substrate than an interface between the top one of the
semiconductor layers and the base layer.
12. The apparatus of claim 8, wherein one of the two of the semiconductor
layers is a doped region of the substrate.
- 25 13. The apparatus of claim 8, further comprising:
a semiconductor extension to the top one of the layers, part of the extension of
the base layer being located between the substrate and the extension of the top one of
the layers.